Design of Direct Digital Synthesizer (DDS) Based on Field Programmable Gate Array (FPGA) for Electrical Impedance Tomography (EIT)

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Intisari — Direct Digital Synthesizer (DDS) memainkan peran penting dalam pembangkitan sinyal presisi tinggi untuk berbagai aplikasi seperti di bidang medis dan telekomunikasi. Penelitian ini mengeksplorasi pengembangan sistem DDS berbasis Field-Programmable Gate Array (FPGA), dengan fokus pada optimalisasi akurasi sinyal, efisiensi penggunaan sumber daya, dan tingkat signal-to-noise ratio (SNR). Studi ini mengimplementasikan dua desain DDS pada FPGA: satu berbasis algoritma CORDIC dan lainnya menggunakan pendekatan Look-Up Table (LUT). Komponen utama dari sistem ini meliputi phase accumulator, phase register, dan algoritma perhitungan frekuensi. Kinerja sistem dievaluasi dengan mengukur akurasi keluaran sinyal dan SNR, menggunakan DAC ISL6961IAZ dan RF Transformer PWB2010LC untuk konversi dan transmisi sinyal. Hasil menunjukkan bahwa DDS berhasil menghasilkan frekuensi mendekati target, yaitu 100,4 kHz untuk target 100 kHz dan 498,8 kHz untuk target 500 kHz. Desain berbasis LUT menunjukkan signal fidelity yang lebih baik, dengan pencapaian SNR sebesar 106 dB dibandingkan 92 dB pada desain berbasis CORDIC. Namun, analisis penggunaan sumber daya mengungkap perlu adanya kompromi antara efisiensi sumber daya Logic element dan penggunaan memori: desain CORDIC menggunakan 26% Logic element dan hanya 1% memori, sedangkan desain LUT menggunakan 8% Logic element namun 77% memori. Temuan ini menyoroti pentingnya menyeimbangkan pilihan desain berdasarkan kebutuhan aplikasi yang spesifik terhadap presisi, keterbatasan sumber daya, dan performa sistem.

Kata kunci – Direct Digital Synthesizer (DDS), FPGA, EIT, CORDIC, LUT, SNR.

Abstract — Direct Digital Synthesizer (DDS) systems play a critical role in high-precision signal generation for applications like medical imaging and RF communications. This research explores the development of a DDS system using Field-Programmable Gate Array (FPGA) technology, with a focus on optimizing signal accuracy, resource efficiency, and signal-to-noise ratio (SNR). The study implemented two DDS designs on an FPGA: one based on the CORDIC algorithm and the other using a Look-Up Table (LUT) approach. Key components of the system included a phase accumulator, phase register, and frequency calculation algorithms. The system's performance was evaluated by measuring signal output accuracy and SNR, utilizing the ISL6961IAZ DAC and RF Transformers PWB2010LC for signal conversion and transmission. The results showed that the DDS achieved near-target frequencies, with outputs of 100.4 kHz for a target of 100 kHz and 498.8 kHz for a target of 500 kHz. The LUT-based design demonstrated superior signal fidelity, achieving an SNR of 106 dB compared to 92 dB for the CORDIC-based design. However, resource utilization analysis revealed a trade-off between logic efficiency and memory usage: the CORDIC design consumed 26% of logic elements and only 1% of memory, while the LUT-based design used 8% of logic elements and 77% of memory. These findings highlight the importance of balancing design choices based on application-specific requirements for precision, resource constraints, and performance.

Keywords – Direct Digital Synthesizer (DDS), FPGA, EIT, CORDIC, LUT, SNR.

I. INTRODUCTION

Electrical Impedance Tomography (EIT) is a non-invasive medical imaging technique that utilizes the measurement of electrical impedance in tissues within the body to visualize the distribution of electrical conductivity [1] The primary advantage of EIT is its ability to provide real-time imaging with portable, easily accessible equipment, at a relatively low cost, and without exposure to harmful radiation, compared to other medical imaging techniques such as MRI or CT scans [2]. EIT has been widely used for monitoring biomedical processes, such as sodium visualization in the skin [3], gastric organ imaging [4], breast cancer [5], neural activity [6], and brain imaging [7].

However, the development of EIT devices still faces several challenges, one of which is in terms of frequency precision and data acquisition speed [8]. A key component in EIT systems is the Direct Digital Synthesizer (DDS), which its functions is to generate the frequency signals required for impedance measurement [9]. Although conventional DDS has been used in EIT applications, there is a need to develop more efficient and precise DDS designs, especially for high frequencies. Additionally, a major challenge of EIT in medical practice is the low frequency injection and the limitation in scanning speed, which requires a long time. Therefore, our research proposes the "Development of a Direct Digital Synthesizer (DDS) Design Based on Field Programmable Gate Array (FPGA) for Electrical Impedance Tomography (EIT) Systems", combining high-frequency injection and high scanning speed solutions to address the main obstacles associated with EIT implementation in clinical environments.

Currently, DDS have been widely used in various applications, but research on the development of DDS specifically for EIT applications, particularly at high frequencies, is still limited. Among the DDS system developments for EIT is the Multi-node Electrical Impedance Tomography (MnEIT), which was developed based on the AD9833 signal generator IC. The results showed that the relative error in amplitude measurement was quite small, at 2.42%, but the usable frequency range was limited to 100 Hz - 100 kHz [10].

The novelty of this research lies in its innovative integration of FPGA technology as both the main controller and the foundation for a DDS specifically optimized for EIT applications. By prioritizing precision and measurement speed which are critical requirements for EIT system, this work leverages FPGA's inherent advantages, such as parallelism, high-speed processing, to develop tailored solutions that enhance measurement quality, system flexibility, and responsiveness [11], [12]. These improvements aim to advance the understanding of electrical impedance phenomena while addressing the technical demands of real-world EIT implementations.

To achieve this, the study implemented two FPGA-based DDS architectures: one using the CORDIC (Coordinate Rotation Digital Computer) algorithm and the other employing a Look-Up Table (LUT) approach. Core components such as a phase accumulator, phase register, and frequency calculation algorithms ensured precise signal generation. Performance evaluation focused on signal accuracy and signal-to-noise ratio (SNR), utilizing the ISL6961IAZ DAC (digital-to-analog converter) and RF Transformers PWB2010LC for signal conversion and transmission. The FPGA's ability to balance computational efficiency (via CORDIC) and rapid data retrieval (via LUT) underscores its suitability for generating high-frequency signals with optimal performance, making it a robust platform for advancing EIT system capabilities.

II. METHODOLOGY

A. *Research Stage*

The research methodology is divided into following steps:

- Literature Review: The aim is to thoroughly understand the theories and previous research related to DDS on FPGA for EIT optimization. In this stage, the research problem can be clearly and specifically formulated, and hypotheses can be developed for testing in the study. At least five international journals have been referenced to build a strong theoretical foundation for the FPGA EIT application proposed in this research.
- DDS System Design: Conceptually designing the DDS system, including measurement circuits and algorithms to be used. Developing an experimental plan to measure amplitude and phase difference at various frequencies.
- DDS Implementation on FPGA: Implementing the DDS design on FPGA to produce high-frequency signals and process measurement signals for amplitude and phase difference. Prototyping the DDS and collecting measurement response data.
- DDS Algorithm Optimization: Analyzing the measurement response data obtained to identify potential improvements in accuracy or measurement speed. At this stage, the DDS on FPGA is expected to be capable of generating high frequencies.
- Validation and Calibration: Conducting validation tests to ensure that the DDS system on FPGA provides consistent and reliable results and performing system calibration to adjust and enhance measurement accuracy.

B. *Direct Digital Synthesizer*

Development method for the DDS is carried out in two stages: DDS configuration and DDS integration. DDS configuration involves designing the internal structure of the FPGA and determining parameters such as sample frequency, data length, and input/output configuration which involves writing code that can calculate amplitude and phase difference to produce input signals at various frequencies, especially high frequencies [13]. While DDS Integration is about design and integration of a DDS system with the DAC and RF Transformers for signal generation in a high-frequency application.

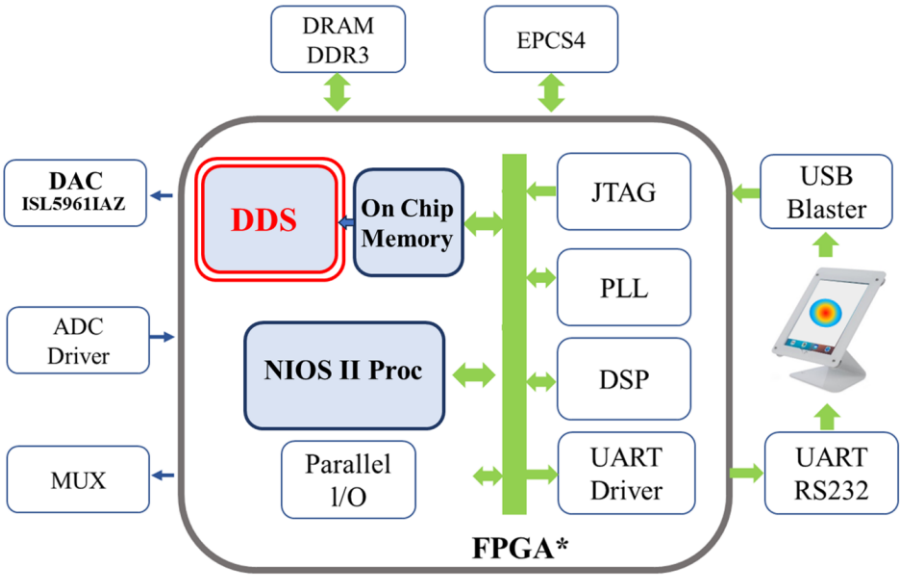

Figure 1. Block diagram of FPGA design

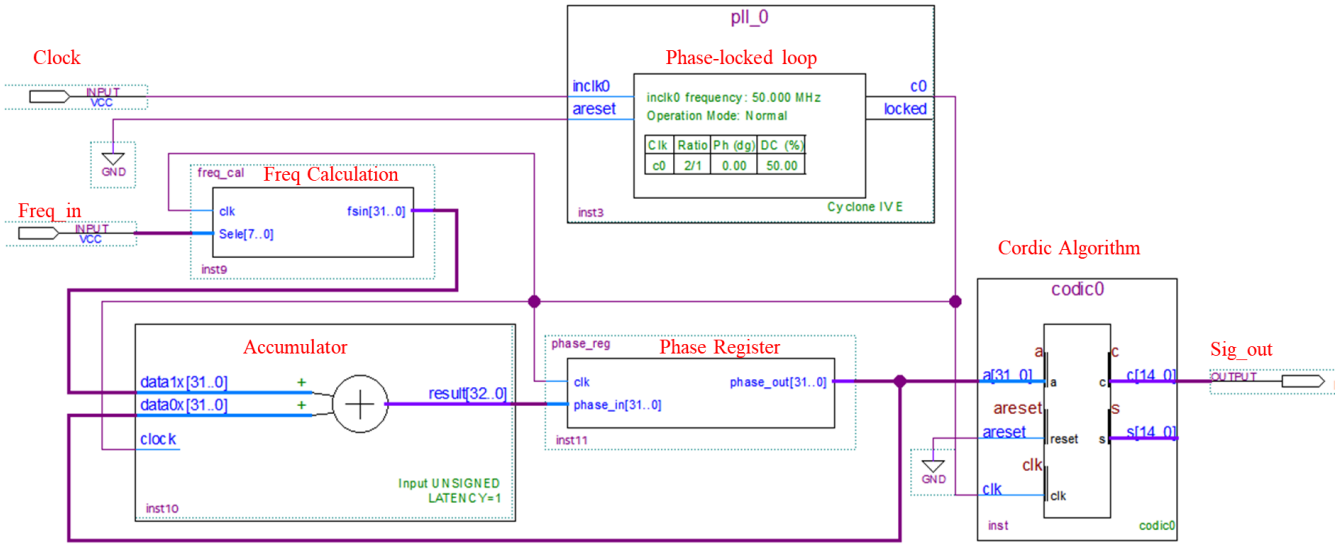

Figure 2. Block diagram of FPGA design

1) *DDS Configuration:* Figure 1 shows the FPGA design, which is created using NIOS II Processor. NIOS II Processor is a reprogrammable processor widely used in FPGA-based system applications. Its primary function is to manage and coordinate the operation of the entire system. In amplitude and phase difference measurements, the NIOS II Processor is used to control the measurement workflow, organize data acquisition, and manage interactions with other components.

DDS is used to generate a sinusoidal wave with a frequency according to the requirements. The DDS system primarily consists of a phase accumulator, a phase modulator, and a sinusoidal ROM lookup table. From here, the output, which is still in digital form, will be converted into an analog signal by a DAC, and then smoothed using a low-pass filter. Figure 2 shows the block diagram of the DDS structure.

Phase-Locked Loop (PLL) is often used in DDS systems to stabilize and multiply the reference clock frequency, ensuring a stable high-frequency clock signal that drives the DDS. It helps synchronize the output frequency with an external reference, improving signal stability.

The output frequency of the DDS is determined by the binary input *M* which is loaded into a frequency register. Here this research needs a Frequency Calculation (for Register Based on n-bit Phase Accumulator). This output value is used in the phase accumulator to step through the phase of the waveform. The formula for output frequency is in (1).

$$f_{out} = \frac{M f_c}{2^n} \quad (1)$$

where f_{out} is the output frequency of the DDS, *M* is the binary input, f_c is the reference clock frequency, and *n* is the total length of the phase accumulator (in bits). In this research we use an n-bit phase accumulator = 32, an M value of 0000...0001 will cause the phase accumulator to overflow after 2^{32} clock cycles. If the M value is changed to 0111...1111, the phase accumulator will overflow after only 2 clock cycles (the minimum value required based on Nyquist). For example, in order to generate sine wave with frequency f_{out} 1 MHz, PLL frequency f_c = 100 MHz, and 32-bits phase accumulator will get M= 42949673.

The phase accumulator is a key part of the DDS system. It increments its value based on the input frequency word *M* and the clock signal. The accumulated phase is used to address a lookup table that contains values for the waveform (typically sinusoidal). The phase accumulator determines the phase progression of the output waveform.

Phase Register is to holds the current phase value, which is updated every clock cycle by the phase accumulator. It stores the phase information, which is then used to retrieve the corresponding amplitude values from the lookup table.

The study implemented two FPGA-based DDS architectures: one using the CORDIC (Coordinate Rotation Digital Computer) algorithm and the other employing a LUT approach. The CORDIC algorithm is often used in DDS to efficiently compute trigonometric functions like sine and cosine without needing large lookup tables. It can be used to generate sine waves in real-time, reducing memory usage while maintaining accuracy, especially when the system requires a dynamic phase shift or when phase modulation is involved [14]. The other dds architecture is a LUT approach. LUT stores precomputed values of the sine and cosine functions for a set of discrete phase points. During operation, the phase accumulator output is used as an index to retrieve the corresponding sine or cosine value from the table. Typically, LUTs are stored in memory or ROM [15].

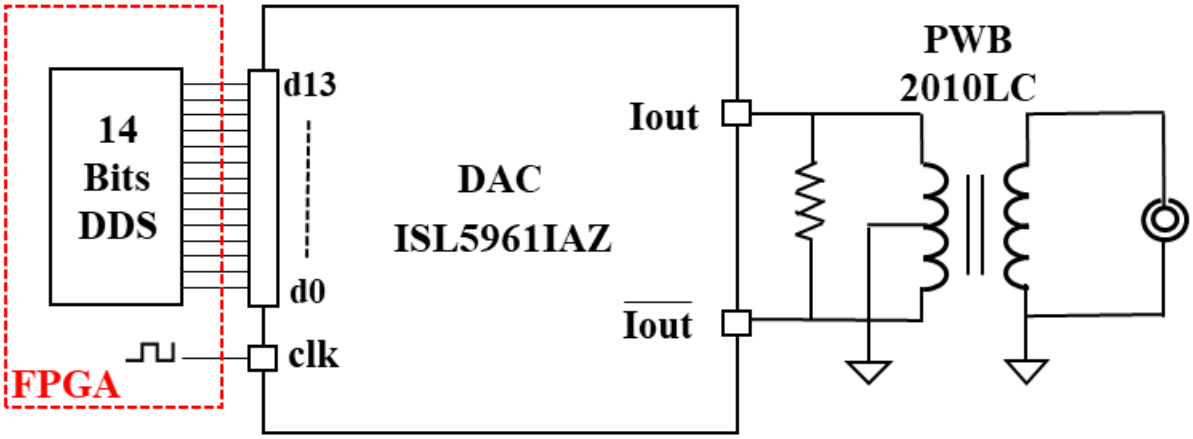

Figure 3. DDS integration with DAC and RF transformer

2) *DDS Integration:* The DDS system generates a sinusoidal waveform with a user-defined frequency, phase, and amplitude. Figure 3 shows DDS Integration with DAC and RF Transformer. The digital waveform generated by the DDS needs to be converted into an analog signal, which is achieved using ISL6961IAZ DAC. Following the DAC stage, the PWB2010LC RF transformer is used to perform impedance matching and provide the appropriate signal transformation for RF applications.

The DDS output, which is in a digital format, is converted into an analog waveform by the ISL6961IAZ. The high-speed nature of this DAC ensures that the frequency and phase information from the DDS is accurately translated into the analog domain. The ISL6961IAZ is a high-speed DAC that provides high precision for analog signal generation, wide output bandwidth, low noise and distortion. This characteristic is ideal for communication and signal processing applications.

The PWB2010LC is connected to the output of the ISL6961IAZ DAC to provide impedance matching between the DAC and the EIT, improving signal quality and transmission efficiency. The PWB2010LC is a RF transformer designed to operate in wide-range frequencies which is critical in ensuring the signal is transmitted efficiently without reflections or signal loss.

III. RESULTS AND DISCUSSION

A. Signal Accuracy

The DDS system was tested to generate signals at two target frequencies. Figure 4 shows signals measurement at frequencies 100 kHz and 500 kHz. When set to 100 kHz, the actual signal measured on the oscilloscope was 100.4 kHz. For the 500 kHz target, the measured signal was 498.8 kHz.

These slight deviations are typical in DDS systems and can be attributed to factors such as clock jitter, finite resolution of the phase accumulator, quantization errors during digital-to-analog conversion, and tolerances in the electronic components. Clock Jitter or Phase Noise is slight variations in the reference clock's stability. Even small amounts of jitter can introduce slight deviations in the output signal. While Finite Resolution of Phase Accumulator means DDS resolution is determined by the number of bits used. If the frequency tuning word cannot exactly match the desired frequency due to limited resolution, small errors occur.

Despite these minor discrepancies, the system exhibits a high level of accuracy, with errors of only 0.4% at 100 kHz and 0.24% at 500 kHz. These error levels fall within acceptable limits for most practical applications [16].

B. Cordic vs Lookup Table (LUT)

DDS both cordic and LUT are implemented on FPGA Cyclone IV E, EP4CE6E22C8 with software Quartus Prime Version 18.1.0 Lite Edition. Tabel 1 shows the resource usage differences between CORDIC and LUT.

The resource usage differences between the CORDIC algorithm and the LUT in a DDS implementation on an FPGA can be understood by analyzing how each method operates and the specific hardware resources they require. Logic elements (LEs) in an FPGA represent the basic building blocks used toperform logic operations like addition, subtraction, and shifting. CORDIC performs iterative computations for each sine and cosine value using shift and add operations. Each step involves performing multiple arithmetic operations, which requires a larger number of logic elements to implement. The complexity grows as the resolution and precision of the output increase, leading to more logic element consumption (1632, or 26% of total LEs). However, since CORDIC calculates values dynamically, it doesn't need to store precomputed values. The only memory usage is for intermediate variables, making it very memory-efficient (86 bits, or <1% of total memory).

Tabel 1. The resource usage between CORDIC and LUT

FPGA EP4CE6E22C8	Resources	Cordic Usage	LUT Usage
Total logic elements	6,272	**1,632 [26%]**	**508 [8%]**
Total registers	millions	1,464 [<1%]	364 [<1%]
Total pins	92	15 [16%]	15 [16%]
Total memory bits	27,6480	**86 [<1%]**	**212,992 [77%]**
Multiplier 9-bit elements	30	0 [0%]	0 [0%]
Total PLLs	2	1 [50%]	1 [50%]

The LUT method on the other hand, avoids complex calculations by storing precomputed values of sine and cosine. As a result, it only needs simple logic to fetch these values from memory and output them, which significantly reduces the need for logic elements (508, or 8% of total LEs). But LUT stores all the necessary waveform data ahead of time, which requires a large amount of memory. The size of the LUT is proportional to the precision of the DDS output. The higher the resolution and frequency precision required, the larger the lookup table, resulting in extensive memory usage (212,992 bits, or 77% of total memory).

C. Signal to Noise Ratio (SNR)

The SNR is a critical metric for evaluating the quality and performance of the generated signal [17]. It represents the ratio between the desired signal (useful information) and the unwanted noise (distortion or errors), and it is usually expressed in decibels (dB) as (2),

$$\text{SNR} = -20\log\left(\frac{\psi}{\mu}\right) \quad (2)$$

where ψ is average noise floor, and μ is the value of measured voltage at injection frequency. In DDS applications, SNR is directly linked to the clarity, accuracy, and usability of the signal for real-world applications.

Figure 5 shows the SNR measurement between LUT and Cordic. Based on signal measurements, the CORDIC algorithm produced a signal with a SNR of 92 dB, while the LUT method resulted in a signal with an SNR of 106 dB. The difference in SNR indicates that the lookup table method generates a cleaner signal with less noise compared to the CORDIC algorithm. This is likely due to the fact that LUT-based implementations directly store precomputed values for the waveform, leading to higher precision and fewer computational artifacts. In contrast, the CORDIC algorithm approximates trigonometric functions through iterative calculations, which, although efficient in terms of hardware resources, can introduce minor inaccuracies and contribute to slightly higher noise levels in the output signal. As a result, the LUT method offers superior signal quality, at the cost of increased memory usage, while the CORDIC algorithm is more resource-efficient but may have a lower SNR due to computational limitations.

The choice between CORDIC and LUT for DDS design depends on the specific needs of the application; CORDIC is ideal for systems with limited memory or where FPGA resources are constrained. While it provides adequate performance, the slightly lower SNR might not be suitable for applications requiring very high signal fidelity. While LUT is preferred for applications where signal accuracy is crucial, such as in high-performance RF systems or high-fidelity audio, even though it demands more memory.

In summary, the CORDIC algorithm is more efficient in terms of computational resources, but sacrifices some signal quality, whereas the LUT method provides superior signal quality at the cost of higher memory consumption. The choice

Figure 4. Signals measurement at two target frequencies 100 kHz and 500 kHz

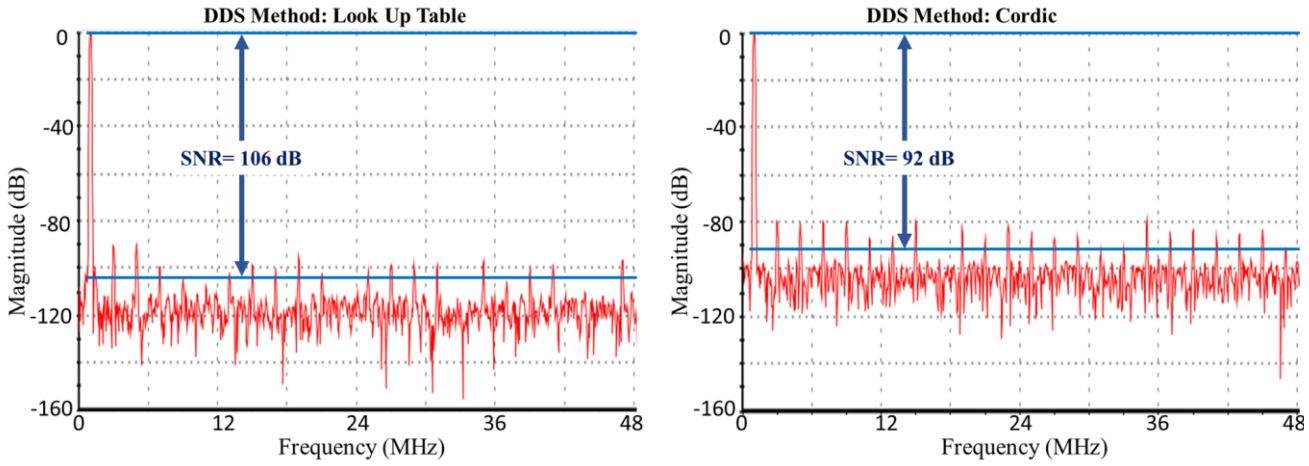

Figure 5. The SNR measurement between LUT and Cordic

between these two methods involves balancing resource availability and desired signal performance.

IV. CONCLUSION

The development of a Direct Digital Synthesizer (DDS) based on Field-Programmable Gate Array (FPGA) technology represents a significant step forward in the area of high-precision signal synthesis. This research demonstrates the successful implementation of two DDS architectures—one based on the CORDIC algorithm and the other utilizing a Look-Up Table (LUT) approach. Both designs achieved high accuracy in generating target frequencies, with only minimal deviations observed. Notably, the LUT-based implementation offered superior signal fidelity, achieving a Signal-to-Noise Ratio (SNR) of 106 dB compared to 92 dB for the CORDIC-based design. However, this improvement came with a trade-off in resource utilization: the CORDIC design consumed 26% of the available logic elements while using only 1% of memory, whereas the LUT-based design required significantly more memory—77% of the total—but only 8% of the logic elements. These results underscore the importance of balancing design choices based on application-specific constraints, particularly in terms of logic efficiency, memory availability, and the required signal quality. The higher SNR achieved by the LUT-based system highlights its potential for applications demanding low-noise and high-precision performance, while the CORDIC-based design remains a viable alternative where logic resources are limited and moderate signal fidelity is acceptable.

FUTURE WORK

At this stage of the research, while the implementation of the DDS in FPGA has shown promising results, there are several areas where further work can be focused to enhance system performance and address some of the current limitations. The DDS implementation, utilizing both CORDIC and LUT algorithms, has demonstrated distinct trade-offs between resource usage and signal quality. Future work can focus on improving the SNR further, particularly for applications that demand extremely high signal fidelity, such as advanced biomedical imaging or high-precision RF systems. This could involve refining the CORDIC algorithm to reduce computational noise or optimizing the LUT size and resolution to further increase the accuracy of signal generation.

The implementation of post-processing filters, such as adaptive or programmable filters, also can be explored to smoothen the output waveform and further reduce spurious noise. This would be particularly useful in mitigating any residual noise introduced by the DAC or imperfections in signal synthesis, leading to cleaner signal generation, especially at higher frequencies.

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